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I. Design Verification

The verification procedure used for SVX4 provides an unbroken chain from logical design to physical implementation. First, designers for each module have simulated their designs under various corner conditions of voltage and foundry transistor performance models. When the required or acceptable performance was achieved, each module was "layout-versus-schematic" (LVS) checked to verify that the physical layout implements the schematic design. Finally, a physical "design-rule-check" (DRC) was run on the modules to verify that there were no violations of the layout rules for the targeted process (TSMC 0.25um Mixed-Signal)*. A presentation of most of these results was given for the SVX4 Final Design Review.

The process outlined above was also performed at each major hierarchy step, i.e. frontend, backend, full-chip, for both SVX4_V1 (baseline version), and SVX4_V2 (on-chip decoupling with single AVDD), with the exception that SVX4_V2 has not been simulated at the schematic level due to its similarity with SVX4_V1. The most advanced design tools available were used, making it possible to run a full-chip schematic simulation using analog simulation methods (Avanti TimeMill/PowerMill simulator). Other simulation tools used were the HSPICE and ELDO analog simulators, and the Cadence Verilog –XL digital simulator. All circuits were simulated with more than one tool, either at the module level, or at a higher level in the hierarchy.

LVS was performed with the Cadence LVS tool, divaLVS, using a layout-extraction rule file modified for use with radiation-tolerant layout techniques and our custom design libraries. For both SVX4 designs, the GDS files submitted for fabrication were streamed back into the Cadence framework for an affirmative LVS check. LVS checking included all transistors, resistors, capacitors, and diodes (except detector input protection), with a 5% size mis-match check for all MOS devices. Physical DRC was performed with a variety of tools, including Cadence (divaDRC, Dracula) and Mentor Graphics (Calibre). The final layout for both versions of SVX4 were cross-checked using two tools capable of handling large designs—at LBNL, Calibre was run before GDS file submission, and at MOSIS the designs were checked with Dracula for confirmation. The procedures described above provide high confidence that the design files submitted for fabrication are logically and physically correct.

* In fact, we accept some known DRC violations related to radiation-tolerant design, and for violations of design rules which have been revised after designs have been successfully fabricated and tested.

II. Circuit Simulations

Vector or Sim Name	Module	Mode	Type	V	Model	RO Freq/ Duty Cyc	Result	Note
SIM_chip	SVX4_V1	CDF	Sch	2.5	TT	26M/50%	Pass	
SIM_chip	SVX4_V1	D0	Sch	2.5	TT	26M/40%	Pass	
sim2_BackEndNew	BackEndNew	CDF	Sch	2.5	TT	26M/50%	Pass	
Inodd3	digCore	N/A	Sch	2.5	TT	50M/50%	Pass	
BN12TN1	digCore	N/A	Ext	2.5	TT	26M/50%	Fail	(1)
BN12TN1	digCore	N/A	Ext	2.5	FF	26M/50%	Pass	
BN12TN1 + rd63	digCore	N/A	Ext	2.5	TT	26M/50%	Pass	
BN12TN1 + rd63	digCore	N/A	Ext	2.25	SS	32M/50%	Pass	
Inodd123	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	
BN12TN1	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	
CTR12	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	(2)
MOD123	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	(2)
PED12345	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	(2)
RN1SP1	digCore	N/A	VXL	2.5	Verilog	26M/50%	Pass	(2)

Type: Sch=schematic simulation, Ext=layout extracted with parasitic capacitance extraction, VXL=Verilog XL
Mode: N/A=all "digCore" simulations are mode-independent

SIM_chip: ReadNeigh, ch 4 over thresh, TN fires after thresh, BN fire before thresh, ch 0-3&5-127 below thresh.

sim2_BackEndNew: ReadNeigh, ch 0 over thresh, TN fires before thresh, BN fires after thresh, ch 1-127 below thresh.

Inodd3: All odd channels except 1, 101, 127 over thresh, ReadNeigh.

BN12TN1: All channels below thresh, ReadSparse with BN and TN fire before thresh; ReadNeigh with TN before thresh and BN after thresh; ReadNeigh with TN and BN after thresh.

Notes: (1) Failure mode is that ch127 data and address are read-out twice; pass with rd63 ON. (2) Detailed descriptions available.

Other: Various layout-extracted analog simulations with parasitics were performed on the pipeline, preamp, ADC, and driver/receivers with corner models and power supply tolerance. This information was largely presented at the SVX4 Final Design Review.

III. Major Specifications (subject to change after fabricated device test)

Dimensions:	9165 um x 6422 um, estimated
Operating Voltage:	2.5 v nom., 2.25 v min., 2.7 v max., all supplies
Absolute Max. Voltage:	3.5 v all supplies*
Operating Current:	AVDD: 60 mA SVDD: 22-160 mA Readout mode DVDD: 20 mA Readout mode (readall) or 9.2 mA Digitize mode, plus 30mA Acquire mode
Operating Frequency:	FECLK: 7.6 MHz @ 20% duty cycle BECLK: 25 MHz Readout mode, 56 MHz Digitize mode @ 40-50% duty cycle
ESD protection:	for detector input pads, diode protection to AVDD/AGND; for all other pads, diode protection to xVDD/AGND with active power supply clamps to AGND

* Could cause permanent analog performance degradation. TBD.